Sentinel LDK

Sentinel HL Chip Form Factor – Technical Specifications Guide

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Sentinel HL Chip Form Factor Technical Specifications Guide

Introduction

Description

Sentinel HL keys protect software against piracy and illegal copying. Access to and execution of the protected software is permitted only when the protected software communicates with the Sentinel HL key. A secure communications channel is established for each communication session between the highly secure, impenetrable AES 128-bit encryption engine on the Sentinel HL key and the application. The secure communication channel between the Sentinel HL key and the application offers powerful resistance to “man-in-the-middle” and brute force attacks. A secure, non external storage device stores licenses, passwords, strings, and application dependent data in its own internal protected read/write memory.

Certain Sentinel HL keys are available using the Sentinel HL Chip form factor. The Sentinel HL Chip is embedded within your device, further enhancing security. This technical specifications guide describes the physical characteristics of the Sentinel HL Chip form factor.

The Sentinel HL Chip is compatible with Sentinel LDK v.6.3 and later.

Initial coding (if required) and verification of the Sentinel HL Chip are performed by Gemalto.

Features

- High performance, low power SmartCard chip
- Operation Ranges: from 4.5V to 5.5V
- Full-speed USB 2.0 interface, embedded pull-up resistor
- ESD Protection to ±2000V(Clock pin), 4000V(LED pin) and 6000V (USB interface pin)
- Hardware AES Engine
- AES/ECC based Secure Tunnel
- Unique serial number for each chip
- Standard SOIC8 Package (RoHS compliant)

Sentinel HL Chip

SOIC8

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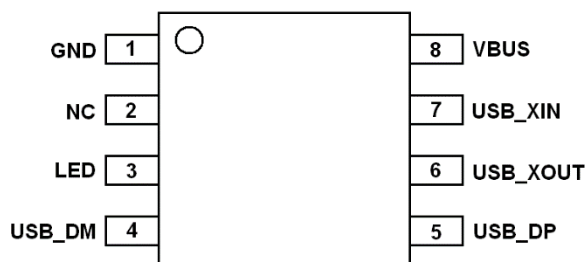
Security

- Dedicated hardware for protection against SPA/DPA/SEMA/DEMA attacks
- Advanced protection against physical attack, including active shield
- Environmental protection systems(voltage, frequency, temperature, light monitors …)
- Secure memory management/access protection (supervisor mode)

Pin Configuration



Pin Number	Pin Name	Description
Pin 1	GND	Ground (reference voltage)
Pin 2	NC	
Pin 3	LED	LED drive, Low level to light the LED
Pin 4	USB_DM	USB D- differential data
Pin 5	USB_DP	USB D+ differential data
Pin 6	USB_XOUT	XTAL output
Pin 7	USB_XIN	XTAL input
Pin 8	VBUS	Power supply input

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Characteristics

Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{BUS}	-0.3	7.5	V
Input Voltage	V_{IN}	Vss-0.3	V_{BUS} +0.3	V
Operating Temperature	T_A	-25	+85	℃
EEPROM Endurance for Write/Erase Cycles	E_{EEPROM}		1 Million	Cycles
EEPROM Data Retention Virgin	$V_{DataRetention}$		10	Years
Electrostatic Discharge (HBM)	ESD		2(Clock pin) 4(LED pin) 6(USB pin)	kV
Latch-up			+/- 200	mA

AC/DC Characteristics

Table 2: AC/DC Characteristics (Condition: VBUS= 4.5V to 5.5V; T=-25℃ to +85℃)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{BUS}	Supply Voltage	4.5	5.0	5.5	V
V_{OH}	Output High Voltage of Pin_LED	0.7*V_{BUS}		V_{BUS}	V
V_{OL}	Output Low Voltage of Pin_LED	0		0.08*V_{BUS}	V
f_{CLK}	CPU Frequency (internal)	28	33	38.5	MHz
$I_{CC\ Run\ Mode}$	Supply Current in Run Mode			10	mA
$I_{CC\ Power\ Down}$	Supply Current in Power Down Mode			400	uA

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Internal Oscillator Characteristics

The internal oscillator is optimized for a 48 MHz ceramic resonator oscillator.

Table 3: Internal oscillator characteristics (T=-20°C to +85°C)

Code	Parameter	Condition	Min.	Typ.	Max.	Unit
Vdd	Supply voltage		1.4	1.8	2.0	V
ΔVdd	Supply ripple	rms value,10kHz to 10MHz			30	mV
Idd on	Current consumption	External capacitors:12pF		4.8	7.1	mA
F_{USB}	Operation frequency for USB			48		MHz
Duty	Duty cycle		40		60	%
Ton	Startup time				1	ms
Pon	Drive level				500	µW
ESR	Equivalent series resistance	@48 MHz			70	Ω
Cm	Motional capacitance	@48 MHz	10		200	pF
Cshunt	Shunt capacitance				6.2	pF
Cload	Load capacitance	Max external capacitor:12pF	2		6	pF
Ldd stdby	Standby current consumption				1	µA

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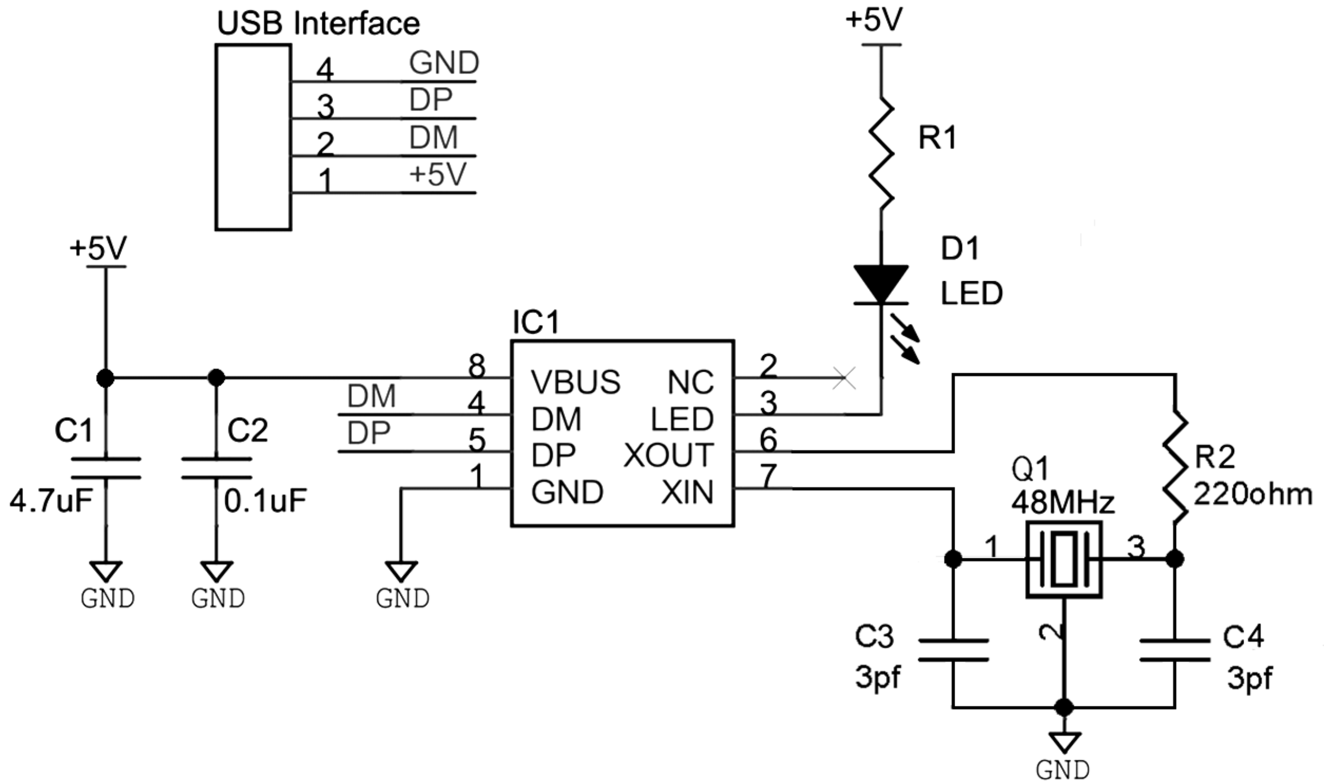
Reference Design

Reference Schematic



Recommended BOM

Ref.	Description	Quantity	Manufacture P/N	Manufacturer
IC1	Sentinel HL Chip	1		Gemalto
Q1	48MHz crystal resonator, ±100ppm, Load Capacitance 6.0±0.1pF	1	XRCGB48M000F0L00R0	MURATA
C1	CAP, 4.7uF, X5R,16V, 0805	1	——	——
C2	CAP, 100nF, X5R, 10V, 10%, 0402	1	——	——
D1	LED, SMD, RED, 0603,	1	——	——
R1	Note(1)	1	——	——
C3,C4	CAP,3pf,COG,50V,0402	2	——	——
R2	Resistor,220Ω,1/16W,1%,0402	1	——	——

Note (1): The parameters of the series resistor depend on the parameters of the LED actually applied.

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Recommend PCB Layout

USB Signal

1. Place the Sentinel HL Chip on the signal layer adjacent to the GND plane.
2. Route D+ and D– on the signal layer adjacent to the GND plane.
3. Route D+ and D– before other signals.
4. Applying the ESD protection chip with Low capacitance TVS array could improve the ESD Immunity level on USB Signals.
5. Keep the GND plane solid under D+ and D–. Splitting the GND plane underneath these signals introduces impedance mismatch and increases electrical missions.
6. Avoid routing D+ and D– through vias; vias introduce impedance mismatch. Where vias are necessary, keep them small (25-mil pad, 10-mil hole) and keep the D+ and D– traces on the same layers.
7. Keep the length of D+ and D– as short as possible.
8. Match the lengths of D+ and D– to be within 50 mils (1.25 mm) of each other to avoid skewing the signals and affecting the crossover voltage.
9. Keep the D+ and D– trace spacing, S, constant along their route. Varying trace separation creates impedance mismatch.
10. Keep a 250-mil (6.5-mm) distance between D+ and D– and other non-static traces wherever possible.
11. Use two 45° bends or round corners instead of 90° bends.
12. Keep a minimum of five trace widths between D+ and D– and any adjacent copper pour. When placed too close to these signals, copper pour affects their impedance.

Capacitor

The Capacitors C1 and C2 should be placed as close as possible to the Sentinel HL Chip.

The Capacitors C3 and C4 should be placed as close as possible to crystal resonator Q1 .

Resonator

- The Resonator should be placed as close as possible to the Sentinel HL Chip.
- Do not use the oscillator terminals to drive other circuits.
- Keep the traces from the Resonator to the Sentinel HL Chip short.
- Keep the traces away from D+ and D-.

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ESD Caution

	ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product contains ESD circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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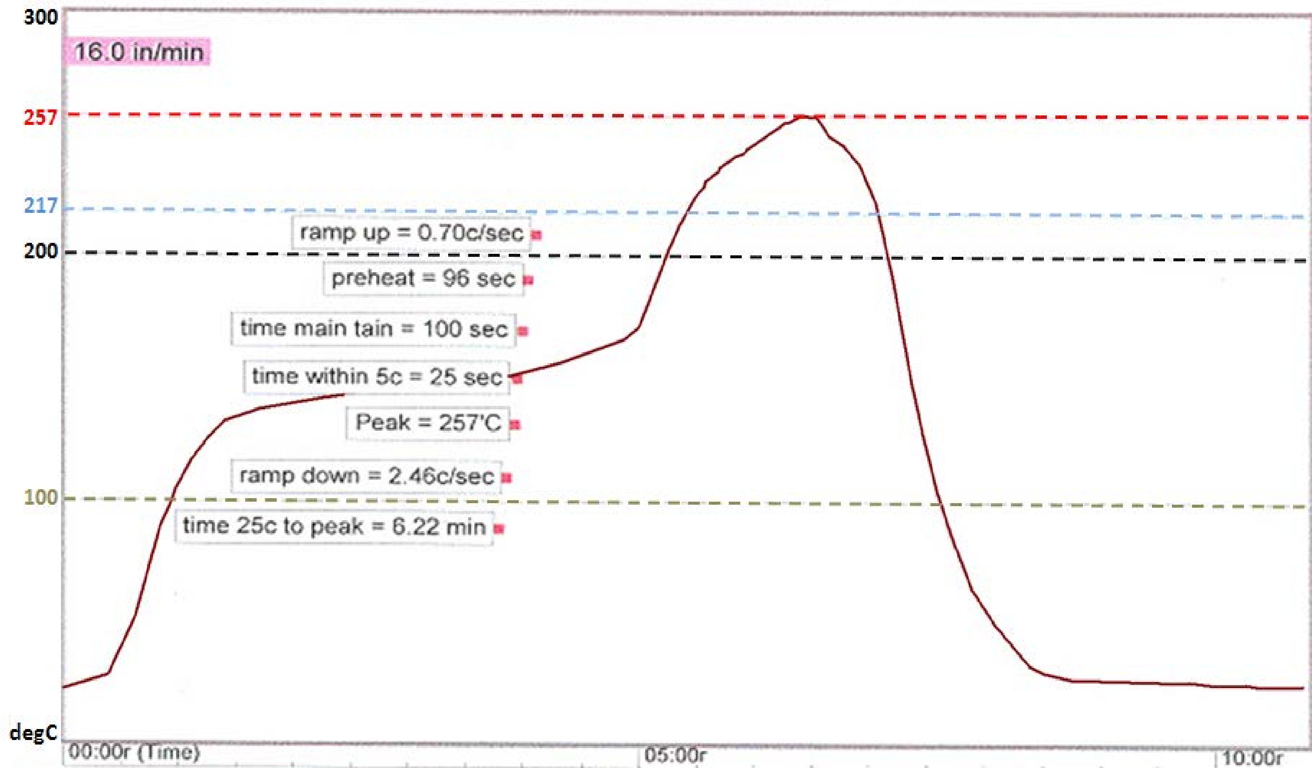
Soldering Reflow Temperature Profile



Parameter	Spec limit per J-STD-020C	Actual Profile
Ramp-Up Rate	3 C/sec Max.	0.70 c/sec
Preheat 150 C to 200 C	60-180 sec	96 sec
Time maintain above 217 C	60-150 sec	100 sec
Time within 5 C of actual Peak	20-40 sec	25 sec
Peak Temperature	255-260 C	257 C
Ramp -Down Rate	6 C/sec Max.	2.46 c/sec
Time 25 C to Peak Temperature	8 minutes Max.	6.22 mins

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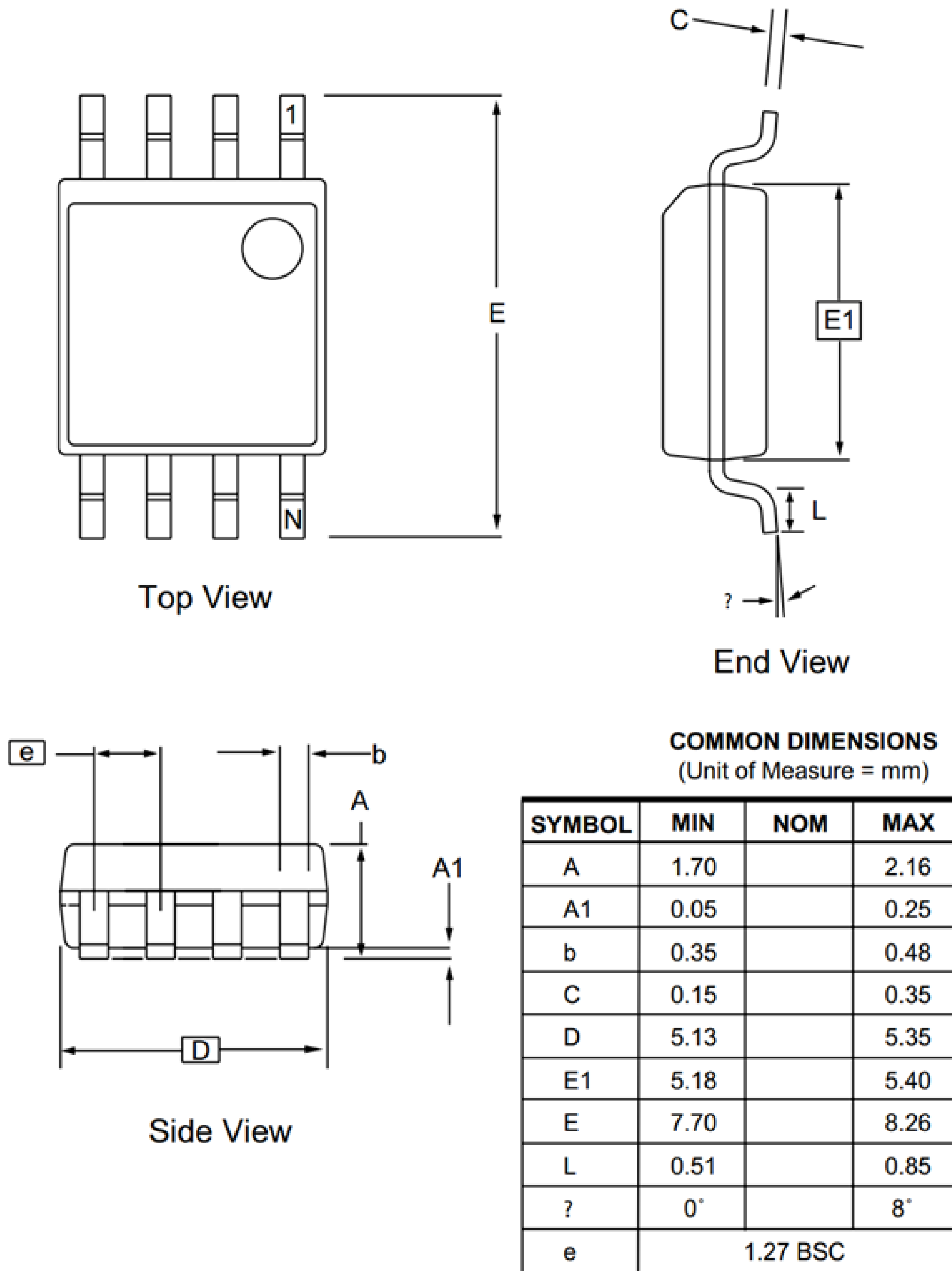
Package Configuration

Figure 1: SOIC-8 Package Characteristics



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX
A	1.70		2.16
A1	0.05		0.25
b	0.35		0.48
C	0.15		0.35
D	5.13		5.35
E1	5.18		5.40
E	7.70		8.26
L	0.51		0.85
?	0°		8°
e	1.27 BSC		

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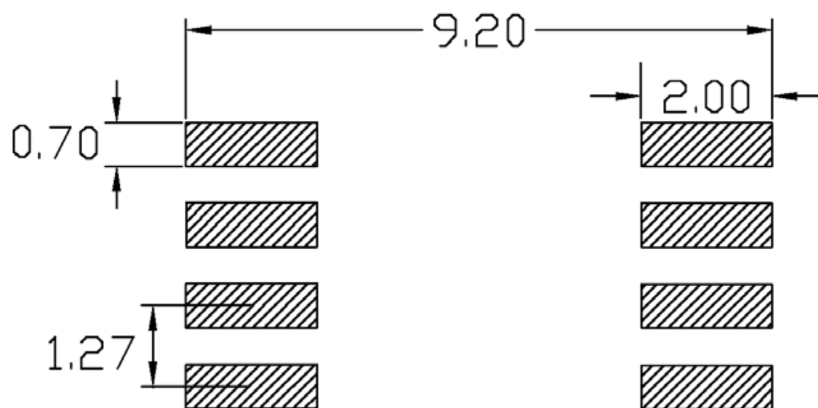
Figure 2: Recommended Footprint (Unit: mm)



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Marking Instruction

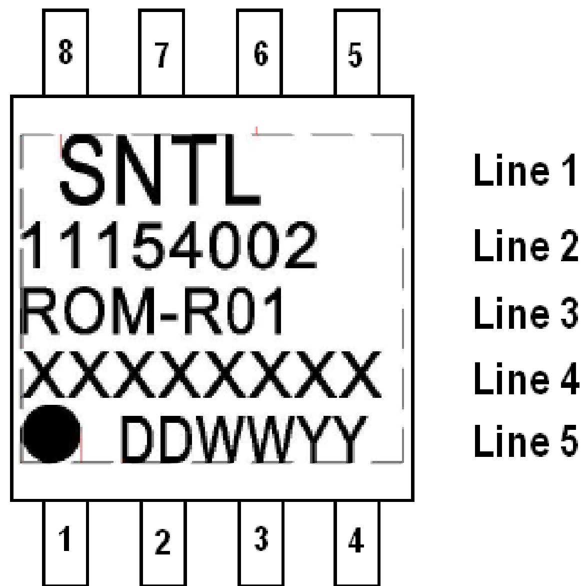

Table 4: Marking Definition

	Comment	Description	Fixed/Dynamic	Alignment	Font Type
Line 1	SNTL	Logo	Fixed	Left	N/A
Line 2	11154002	Gemalto Part Number	Fixed	Left	Arial
Line 3	ROM-R01	ROM Version	Fixed	Left	Arial
Line 4	XXXXXXXX	Lot number	Dynamic	Left	Arial
Line 5	DDWWYY	Production date code	Dynamic	Left	Arial

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Packaging

Sentinel HL Chips are packaged using either of the following systems:

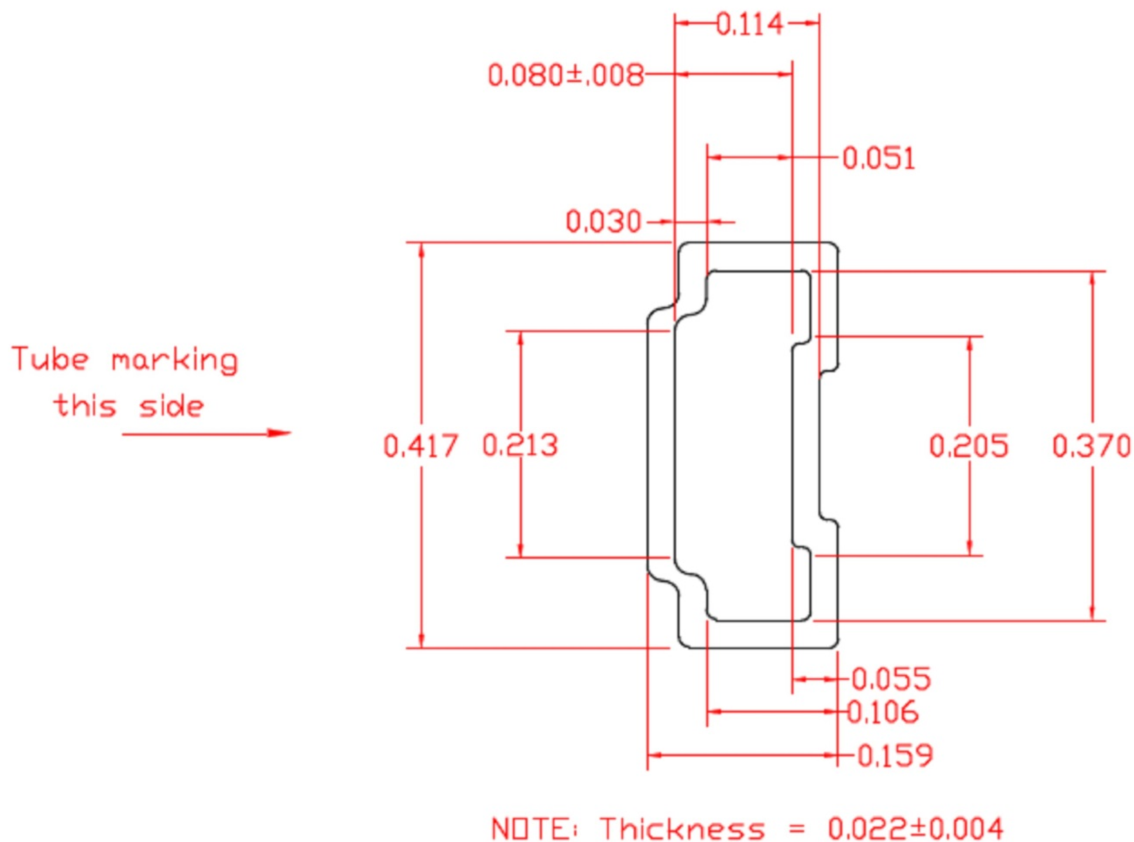
- By default, chips are packaged in tubes that contain 95 chips each.
- Gemalto can provide chips using tape and reel packaging. Each reel contains up to 2,000 chips.

For more information on packaging, contact your Gemalto representative.

Tube Packaging Specifications

A tube packing system protects the IC from damage during shipping and storage and is designed for automatic pick-and-place equipment. Each tube contains 95 chips.

Figure 3: Tube Dimensions



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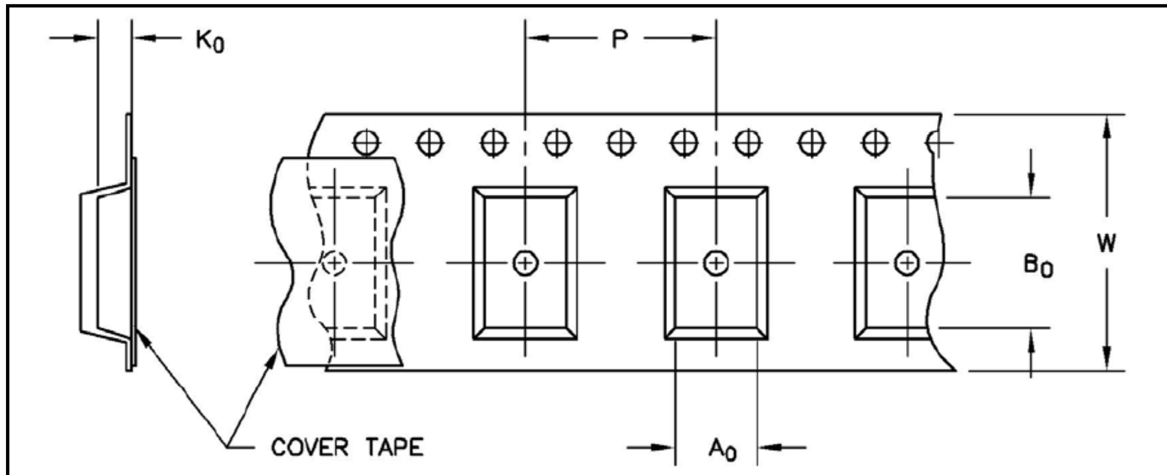
Tape and Reel Packaging Specifications

A tape and reel packaging system protects the IC from damage during shipping and storage and is designed for automatic pick-and-place equipment.

Figure 4: Carrier Tape Dimensions



Carrier Dimensions		Cavity Dimensions			Units Per Reel	Reel Diameter (mm)
W (mm)	P (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)		
16	12	8.6	5.7	2.3	2000	330

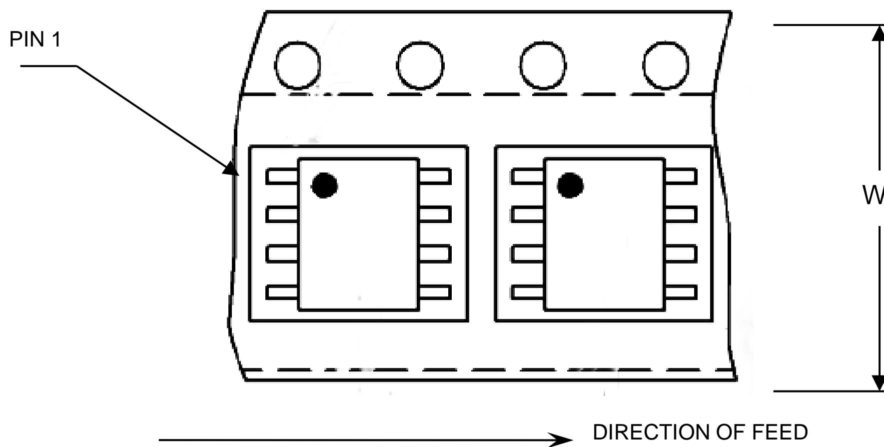


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Figure 5: Device Loading Orientation

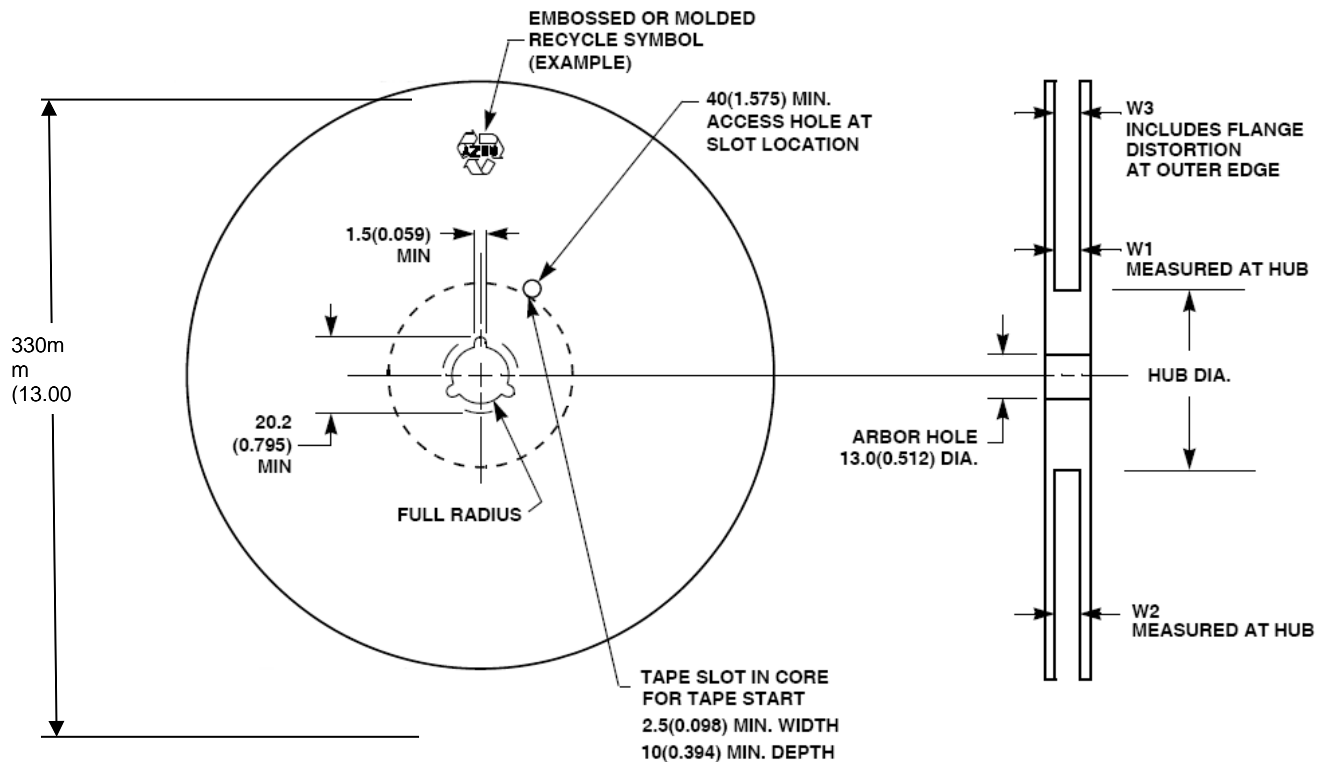

Table 5: Reel Dimensions

WI (NORMAL)	W2 (MAXIMUM)	W3 (MAXIMUM)
16.4 mm	22.4 mm	19.4 mm

Label On Packaging

Human and machine readable labels are provided on each reel, packaging bag and carton box. The contents of each label are listed below:

- P/N: Manufacturer Part Number and Revision
- IPN: Internal (Gemalto) Part Number
- Date Code: Programming Date Code
- IC Lot No.
- Quantity
- COO: Country of Origin
- MSL: Moisture Sensitive Level
- Max. Reflow Temp.: Maximum Reflow Temperature
- Package
- ESD Protection, RoHS compliance, China RoHS LOGO

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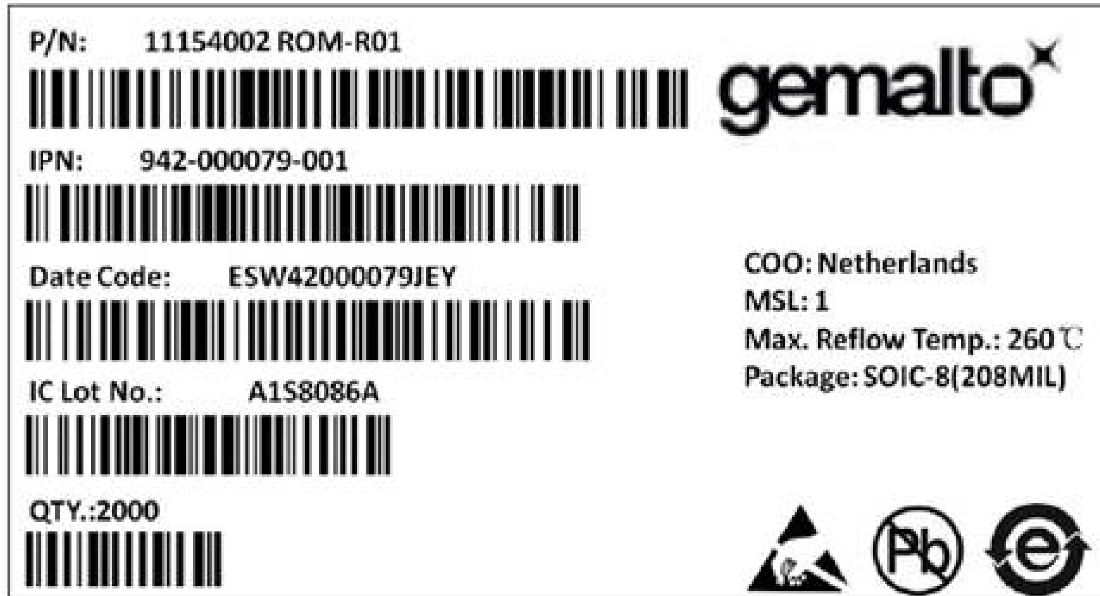
Refer to the figure below for details.

Figure 6: Label on packaging



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